Silicon 2020

2014 update

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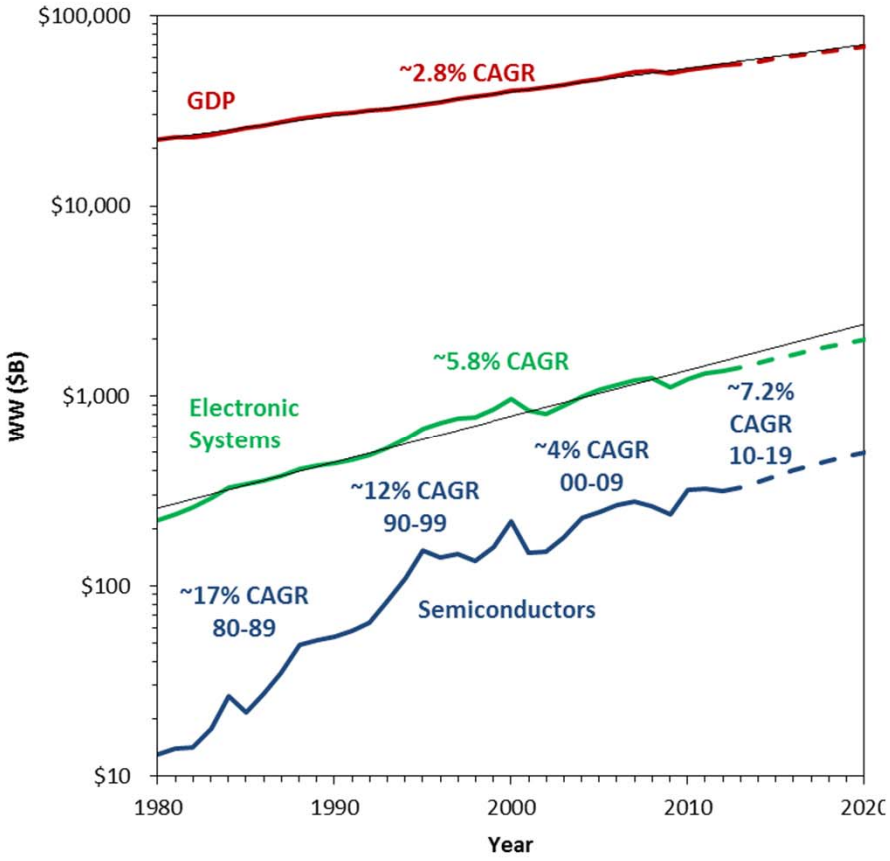
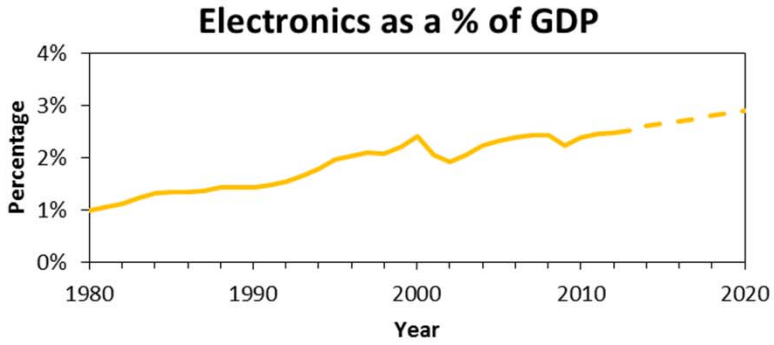
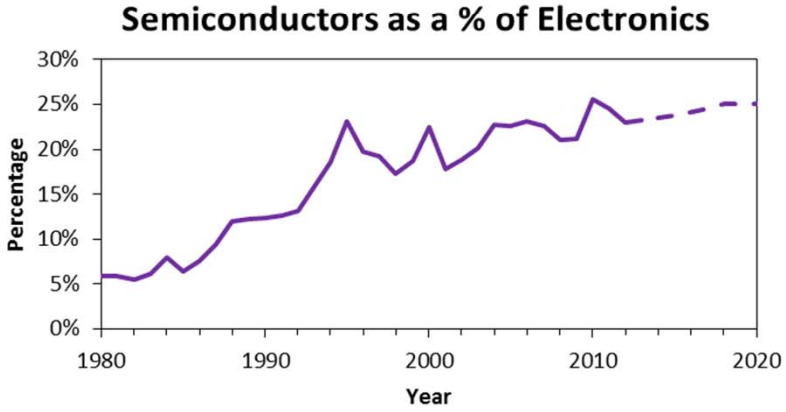
Outline

- Economic Forecast
- Silicon forecast
  - Total MSI
  - By wafer size and year with 2020 profile
  - By wafer type 2020
- Technology trends
  - Memory and Logic trends
  - SOI opportunity
  - High mobility channels
- Conclusion

Worldwide Semiconductor Forecast







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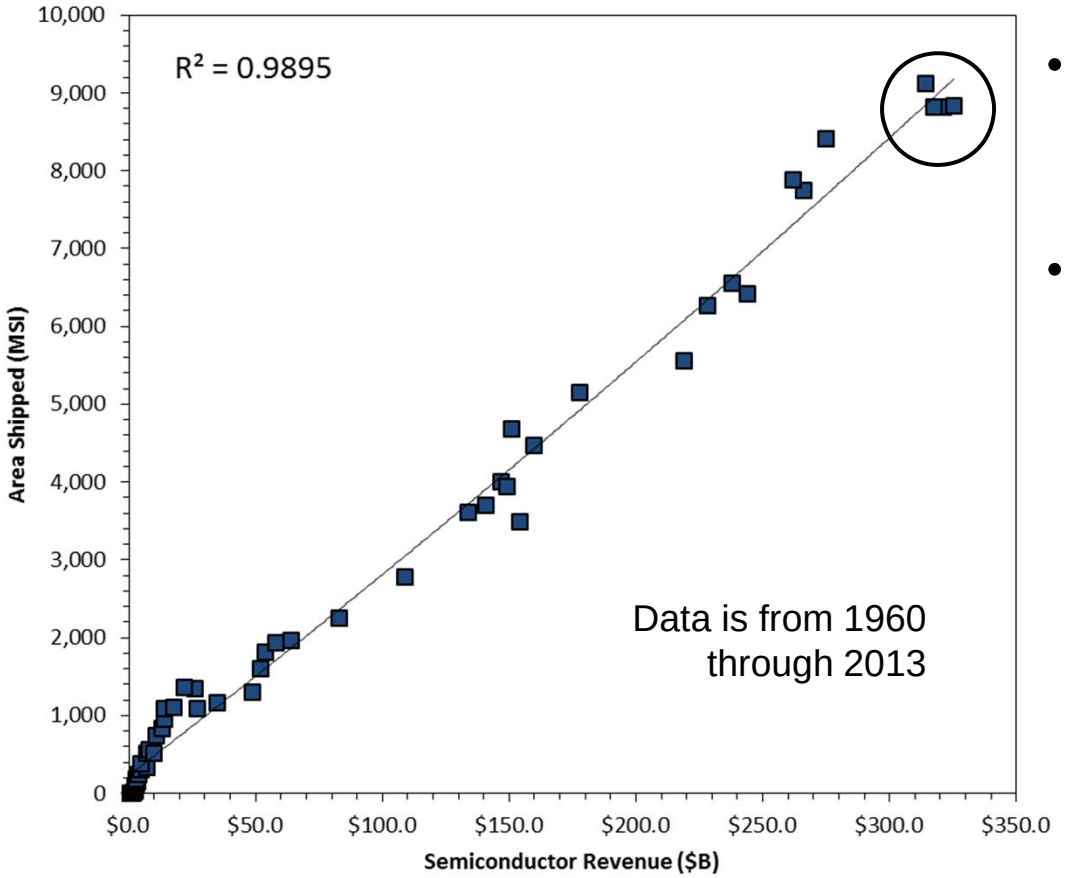
Actual values: GDP per World Bank in constant 2005 dollars, electronics and semiconductor per IC Insights. Forecasts per IC Knowledge.

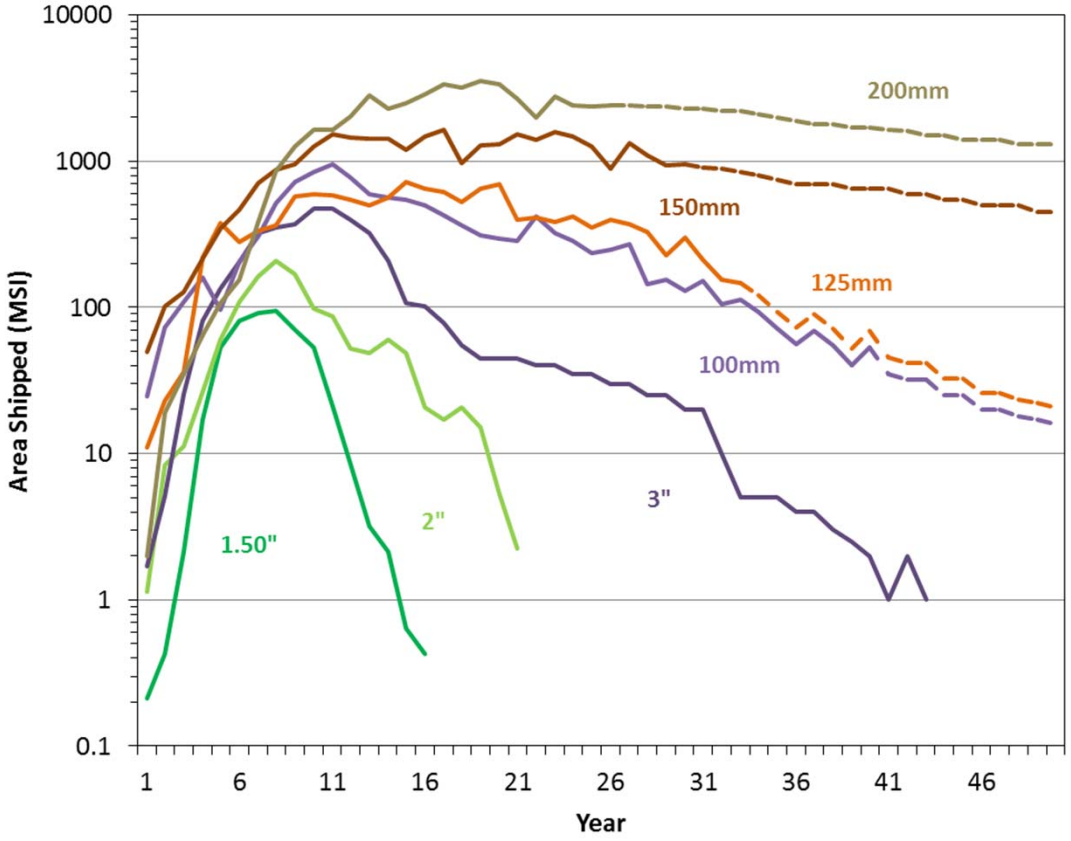
Silicon Versus Semiconductor Revenue



- Worldwide silicon MSI is highly correlated to semiconductor revenue.
- Combining the Worldwide Semiconductor Forecast slide with this slide produces a total silicon MSI forecast.

Semiconductor revenue per IC Insights, MSI per SEMI

Wafer Size Life Cycles



- Each successive generation of wafer size is reaching higher peak shipments, maintaining the peak longer and declining more slowly.

Actual data per SEMI, forecast per IC Knowledge

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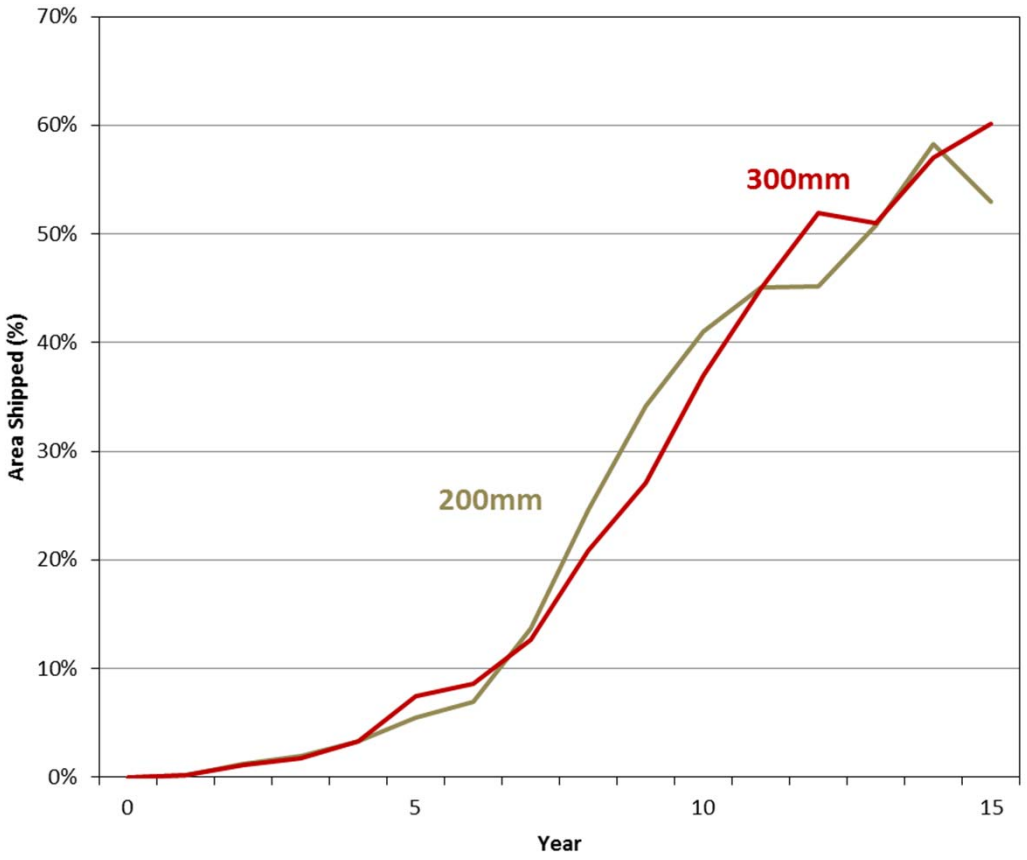
New Wafer Size Ramps



- The ramp up of 200mm and 300mm as a percentage of silicon area shipped has been essentially identical.
- The ramp can be used to forecast the 450mm ramp once a start date is known.
- **A 2020 ramp start is assumed versus 2018 last year.**

Actual data per SEMI

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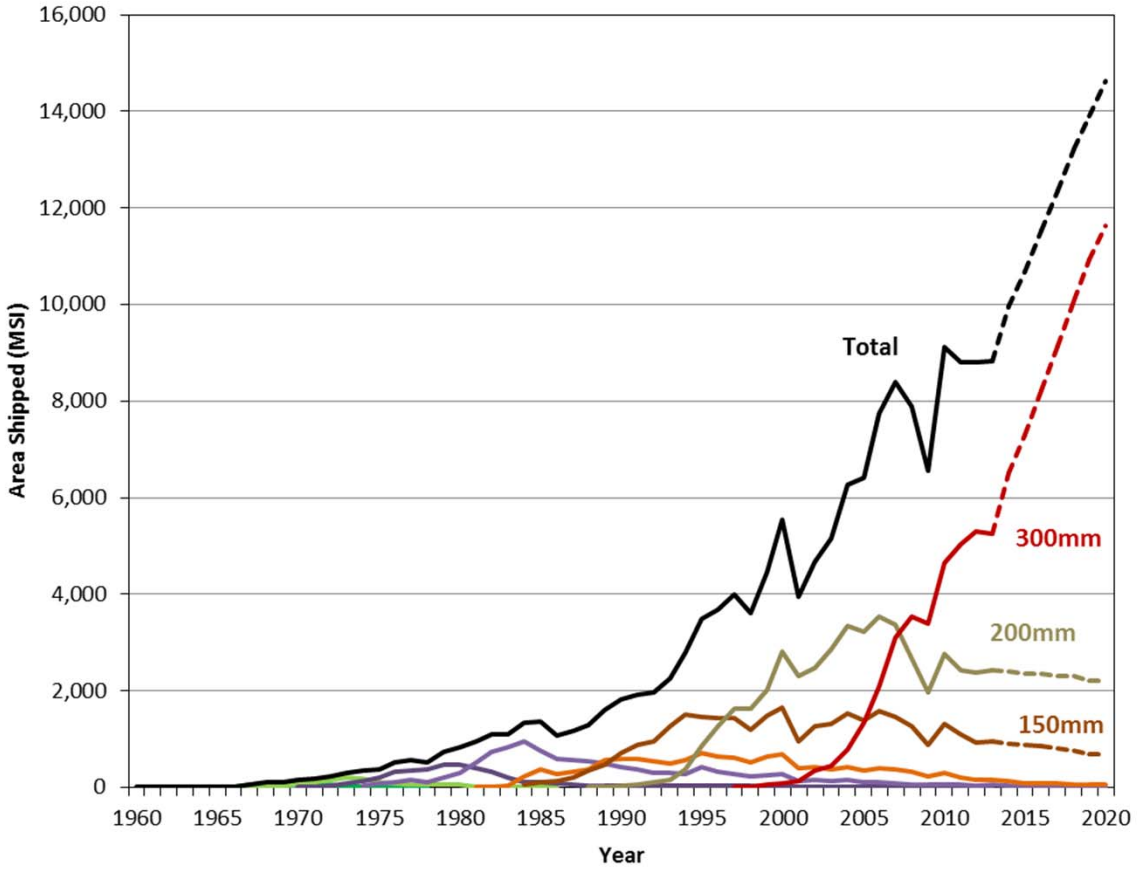
Silicon By Wafer Size Forecast



- Total MSI calculated from the Worldwide Semiconductor Forecast slide and Silicon Versus Semiconductor Revenue slide.
- <300mm decline is per the Life Cycle slide.
- 300mm is the remainder

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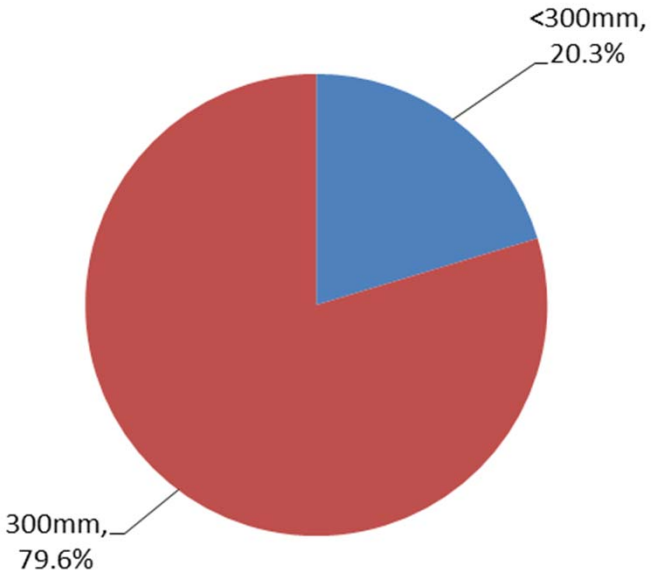
Actual data per SEMI, forecast per IC Knowledge.

Silicon by Wafer Size 2020



- <300mm slowly declining.
- 300mm at the highest percentage seen since the late 1960s.
- **No 450mm versus last year at 3.7%.**

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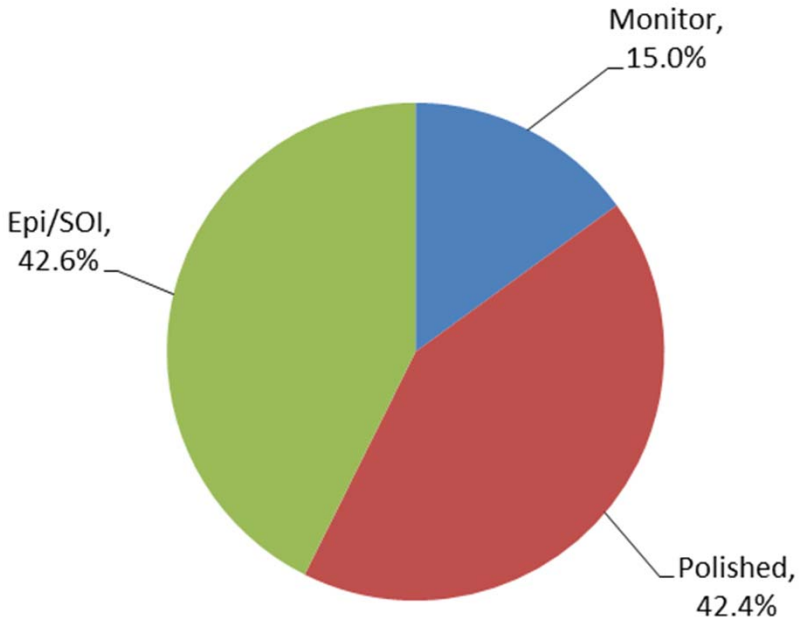
Forecast per IC Knowledge – see the Silicon by Wafer Size slide for background information.

Silicon By Wafer Type 2020



- Raw wafers are used for memory (DRAM/Flash)
- Epi/SOI is used for logic products.
- **Epi/SOI is a higher percentage versus last year.**

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Forecast per IC Knowledge. Includes 300mm wafer size only and represents percentages of MSI

Technology Trends

- DRAM memory cell scaling issues – may transition to MRAM
  - DRAM and MRAM use the same starting wafer type.
- Flash will likely transition from 2D to 3D and long term possibly RRAM
  - in all cases the wafer type stays the same.
  - 3D does potentially drive less wafers.
- Logic is in transition to fully depleted devices now.
  - Fully depleted SOI (FDSOI) - planar
  - Multi-gate
    - Bulk
    - SOI
  - 20nm is the end of bulk planar for logic

How Much SOI?

Device	Relative Cost
FDSOI	1.06
MG – Bulk	1.00
MG – SOI	0.97

Source: IC Knowledge – Strategic Cost Model. Assumes 14nm node processes in the same fab.

- FDSOI – useful for low power applications such as mobile devices but not good for high performance. Also long term scaling issues with layer thickness.
- Multi-gate (MG) can be bulk or SOI. Bulk is the leading solution based on market share.

For more information on this analysis plus an extensive set of industry comments see: https://www.semiwiki.com/forum/content/3599-soi-really-less-expensive.html

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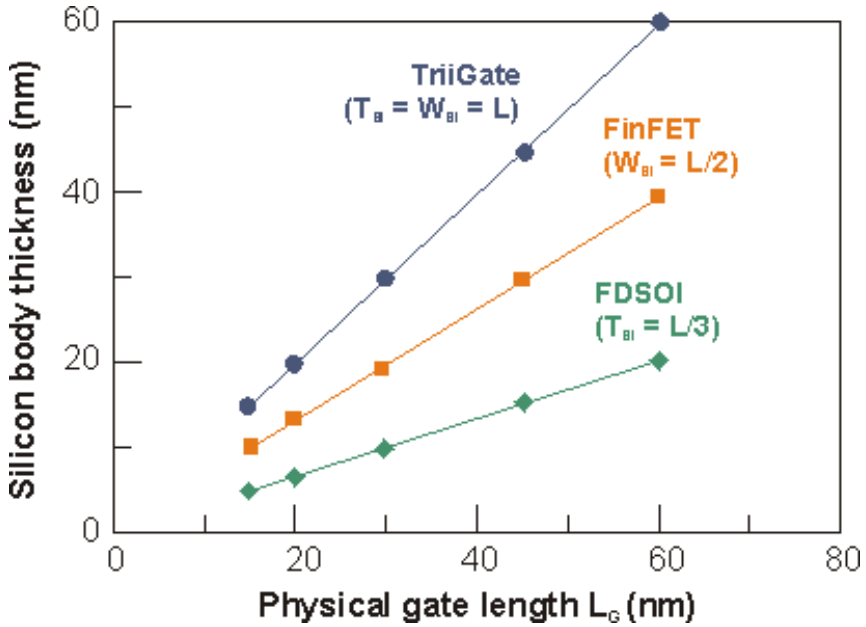
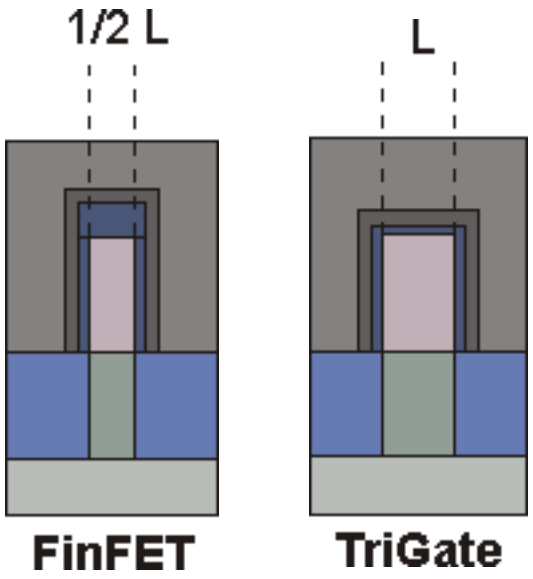
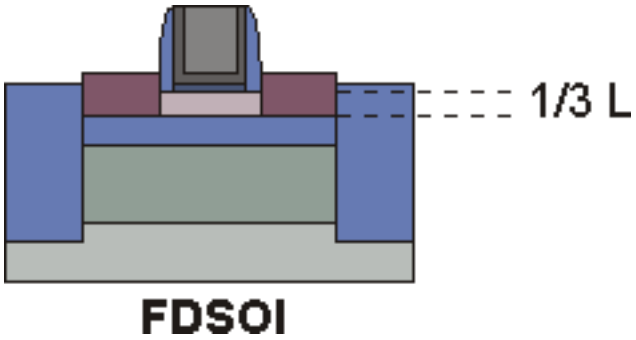
Silicon Thickness Comparison







A TriGate has the most relaxed width/thickness requirement for fully depleted operation.

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14nm/16nm Solutions

Company	Process	Capacity (normalized)
Global Foundries	MG on bulk and FDSOI	0.10/0.01[a]
IBM	MG on SOI (eDRAM driven)	0.02
Intel	MG on bulk	0.27
Samsung	MG on bulk	0.22[b]
ST Micro	FDSOI	0.01
TSMC	MG on bulk	0.36
UMC	MG on bulk	0.01

[a] Could shift based on demand

[b] Has licensed FDSOI at 28nm, currently no announced 14nm FDSOI plans 96% Epi, 4% SOI based on current announcements.

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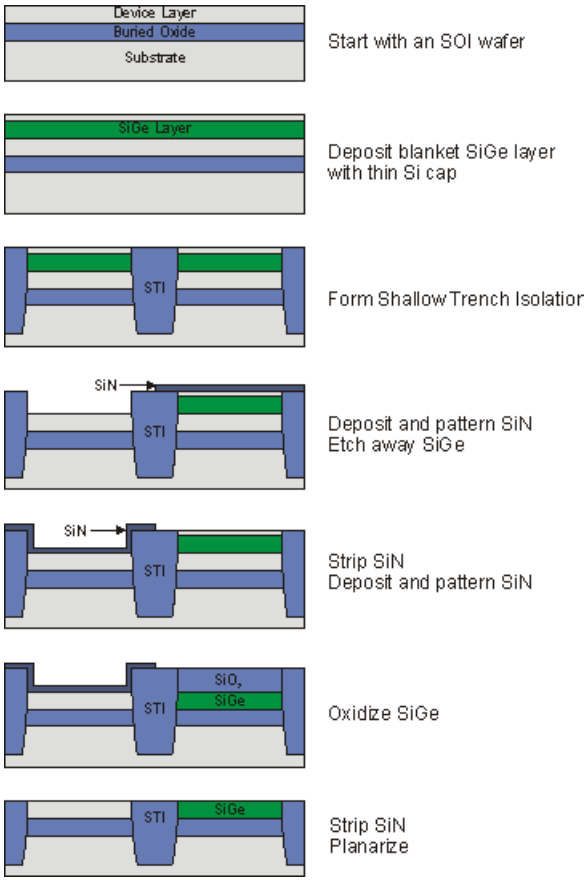
Logic High Mobility Channels

- In order to continue to drive performance we expect both MG and FDSOI to transition to high mobility channels.

Carrier	Si	Ge	InGaAs
Electrons	1,400	3,900	10,000
Holes	470	1,900	250

- SiGe PMOS channels can be created on SOI using the Ge condensation method (announced for 14nm FDSOI).
- Ge and, or InGaAs fins can be created on bulk by selective epitaxial deposition in trenches using aspect ratio trapping.
- In all cases the base substrate remains silicon.

SiGe PMOS by Ge-Condensation



- The process illustrated on the left creates SiGe regions where the PMOS will be fabricated and leaves Si regions where NMOS will be fabricated.
- Oxidation of a SiGe layer over a thin Si layers causes the Ge to diffuse down into the thin Si layer converting it to SiGe and the Si left in the original SiGe layer oxidizes to SiO_2.
- This is called the Ge-condensation technique.
- This technique can be applied to FDSOI or Multigate on SOI to create SiGe channel PMOS.

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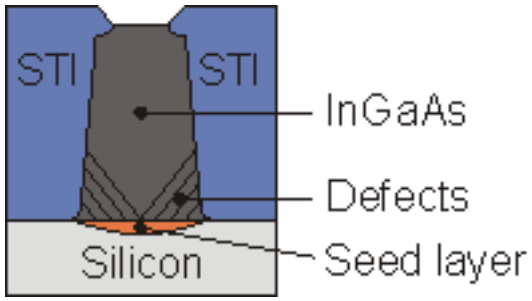
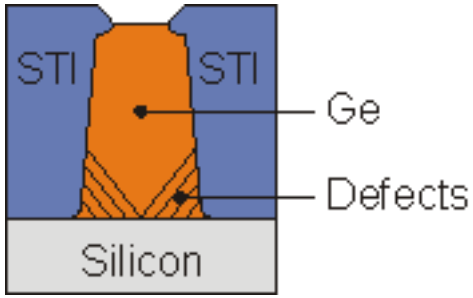
Aspect Ratio Trapping





- Ge and InGaAs have 4% and 8% lattice mismatches to silicon respectively.
- Ge and InGaAs form defects when deposited on silicon.
- InGaAs or Ge layers can be grown in trenches bounded by Shallow Trench Isolation (STI).
- The film threading defects propagate at a 55^{o} angle up from the silicon interface and are trapped by the walls of the STI in the bottom of the trench as long as the aspect ratio of the trench is greater than 1.4.
- InGaAs needs a Ge seed layer to grow on silicon.
- Ge fins at 14nm/10nm, InGaAs fins at 10nm/7nm.

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Conclusion

- Silicon 2020 will be dominated by 300mm, we no longer expect 450mm production in 2020.
- Polished wafers and Epi/SOI will have roughly equal share..
- Logic will be split between Epi and SOI.
- Our current projection is SOI will be only represent about 4% of 14nm demand with a high end of 15%.
- High mobility channels for logic will enter use at 14nm and become widespread by 10nm. The base substrate is still silicon.